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**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

In re the Application of:

Attorney Docket No.: ROH-030

Keiichi DEN

Application No.: 09/702,870

Examiner: L. C. Thai

Filed: November 1, 2000

Art Unit: 2811

For: SEMICONDUCTOR DEVICE OF CHIP-ON-CHIP STRUCTURE WITH RADIATION NOISE SHIELD (as amended)

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**AMENDMENT UNDER 37 C.F.R. §1.111**

Commissioner for Patents  
Washington, DC 20231

Date: March 19, 2002

Sir:

In response to the Office Action dated December 21, 2001, please amend the above-identified application as follows:

**IN THE TITLE:**

Please change the title of the invention to ~~SEMICONDUCTOR DEVICE OF~~  
~~CHIP-ON-CHIP STRUCTURE WITH A RADIATION NOISE SHIELD--.~~

**IN THE DRAWINGS:**

A Request for Approval of Drawing Corrections proposing a red-line corrections to Figs. 3-5 is filed herewith.

**IN THE CLAIMS:**

Please cancel claims 1, 6, 11 and 21 without prejudice or disclaimer.

Please amend claims 2, 4, 7-10, 12-17, 19, 20 and 22-25 as set forth below in clean form. Additionally, in accordance with 37 CFR 1.121(c)(1)(ii), amended claim(s) is/are set forth in a marked-up version in the page(s) attached to this Amendment.

A1

2. (Amended) A semiconductor device as set forth in claim 7, further comprising a connection mechanism which connects the noise shield film to a power supply portion.

A2

4. (Amended) A semiconductor device as set forth in claim 7, further comprising an electrode portion provided between the first semiconductor chip and the second semiconductor chip for electrical connection between the first and second semiconductor chips, wherein the noise shield film is composed of the same material as the electrode portion.

A3

7. (Amended) A semiconductor device comprising:

- a first semiconductor chip;
- a second semiconductor chip bonded onto the first semiconductor chip in stacked relation; and
- a noise shield film provided between the first semiconductor chip and the second semiconductor chip for preventing the first and second semiconductor chips from being mutually influenced by noises thereof,

wherein the first semiconductor chip is greater in size than the second semiconductor chip, and the noise shield film is provided on a surface of at least the first semiconductor chip,

wherein a major noise source is present in the second semiconductor chip,

wherein the noise shield film includes a shield portion which covers an area in which the major noise source is present, and an extension portion extending outwardly from the shield portion on a surface of the first semiconductor chip and beyond an edge of the second semiconductor chip.

8. (Amended) A semiconductor device as set forth in claim 7, wherein the noise shield film is provided in a region which covers a major noise source.

9. (Amended) A semiconductor device as set forth in claim 7, wherein the first and second semiconductor chips are bonded to each other with active surfaces thereof being opposed to each other.

A3  
Cont

10. (Amended) A semiconductor device as set forth in claim 7, wherein the noise shield film includes a metal film provided on a surface of at least one of the first semiconductor chip and the second semiconductor chip.

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A4

12. (Amended) A semiconductor device as set forth in claim 15, wherein the heat radiator includes a heat sink.

13. (Amended) A semiconductor device comprising:  
a first semiconductor chip;  
a second semiconductor chip bonded onto the first semiconductor chip in stacked relation;  
a heat conductive member provided between the first semiconductor chip and the second semiconductor chip to define a heat release path for releasing heat generated by the second semiconductor chip; and  
a connection member thermally connecting the heat conductive member to a heat radiator, the heat radiator including a heat sink wherein the connection member includes a bonding wire which connects the heat conductive member to the heat sink.

14. (Amended) A semiconductor device as set forth in claim 13, wherein the heat conductive member includes a metal film provided on a surface of at least one of the first semiconductor chip and the second semiconductor chip.

15. (Amended) A semiconductor device comprising:  
a first semiconductor chip;  
a second semiconductor chip bonded onto the first semiconductor chip in stacked relation;  
a heat conductive member provided between the first semiconductor chip and the second semiconductor chip to define a heat release path for releasing heat

generated by the second semiconductor chip; and

AG  
cont  
a connection member thermally connecting the heat conductive member to a heat radiator, wherein the heat conductive member includes a metal film provided on a surface of at least one of the first semiconductor chip and the second semiconductor chip,

wherein the first semiconductor chip is greater in size than the second semiconductor chip,

wherein the metal film has an extension portion which extends from the vicinity of the major heat source to a surface portion of the first semiconductor chip not covered with the second semiconductor chip, and the extension portion of the metal film is thermally connected to the heat radiator via the connection member and extends beyond an edge of the second semiconductor chip.

16. (Amended) A semiconductor device comprising:

a first semiconductor chip;

a second semiconductor chip bonded onto the first semiconductor chip in stacked relation;

a heat conductive member provided between the first semiconductor chip and the second semiconductor chip to define a heat release path for releasing heat generated by the second semiconductor chip; and

a connection member thermally connecting the heat conductive member to a heat radiator,

wherein the heat conductive member includes a first metal film provided on a surface of the first semiconductor chip and a second metal film provided on a surface of the second semiconductor chip, and the first metal film and the second metal film are disposed in contact with each other or bonded to each other,

wherein the first metal film is thermally connected to the heat radiator via the connection member.

A4  
C14  
17. (Amended) A semiconductor device as set forth in claim 13, further comprising an electrode portion provided between the first semiconductor chip and the second semiconductor chip for electrical connection between the first and second semiconductor chips, wherein the heat conductive member is composed of the same metal material as the electrode portion.

A5  
19. (Amended) A semiconductor device as set forth in claim 13, further comprising a lead frame,  
wherein the first semiconductor chip is die-bonded to the lead frame.

20. (Amended) A semiconductor device as set forth in claim 13, wherein the first and second semiconductor chips are bonded to each other with active surfaces thereof being opposed to each other.

A6  
22. (Amended) A semiconductor device comprising:  
a first semiconductor chip;  
a second semiconductor chip bonded onto the first semiconductor chip in stacked relation; and  
wherein the first semiconductor chip is greater in size than the second semiconductor chip, and the metal film is provided on a surface of at least the first semiconductor chip,  
wherein a major noise source is present in the second semiconductor chip,  
wherein the metal film includes a shield portion which covers an area in which the major noise source is present, and an extension portion extending outwardly from the shield portion on a surface of the first semiconductor chip and beyond an edge of the second semiconductor chip  
wherein the metal film is provided in a region which covers the major noise source within the second semiconductor chip.

23. (Amended) A semiconductor device comprising:  
a first semiconductor chip;  
a second semiconductor chip bonded onto the first semiconductor chip in stacked relation;  
a metal film provided between the first semiconductor chip and the second semiconductor chip; and  
a connection member thermally connecting the metal film to a heat radiator including a heat sink,  
wherein the connection member includes a bonding wire which connects the metal film to the heat sink and,  
wherein the metal film provides a heat release path for releasing heat from a major heat source within the second semiconductor chip.

24. (Amended) A semiconductor device comprising:  
a first semiconductor chip;  
a second semiconductor chip bonded onto the first semiconductor chip in stacked relation;  
a metal film provided between the first semiconductor chip and the second semiconductor chip, the metal film being provided on a surface of at least one of the first semiconductor chip and the second semiconductor chip; and  
a connection member thermally connecting the heat metal film to a heat radiator,  
wherein the first semiconductor chip is greater in size than the second semiconductor chip,  
wherein the metal film has an extension portion which extends to a surface portion of the first semiconductor chip not covered with the second semiconductor chip, and the extension portion of the metal film extends beyond an edge of the second semiconductor chip,

wherein the metal film is provided in a region which covers a major noise source within the second semiconductor chip, and also provides a heat release path for releasing heat from the major heat source with in the second semiconductor chip.

25. (Amended) A semiconductor device comprising:

a first semiconductor chip;

a second semiconductor chip bonded onto the first semiconductor chip in stacked relation;

a metal film provided between the first semiconductor chip and the second semiconductor chip to define a heat release path for releasing heat generated by the second semiconductor chip;

a connection member thermally connecting the metal film to a heat radiator; and

an electrode portion,

wherein the metal film includes a first metal film portion provided on a surface of the first semiconductor chip and a second metal film portion provided on a surface of the second semiconductor chip, and the first metal film portion and the second metal film portion are disposed in contact with each other or bonded to each other,

wherein the first metal film portion is thermally connected to the heat radiator via the connection member and the electrode portion provided between the first semiconductor chip and the second semiconductor chip for electrical connection between the first and second semiconductor chips,

wherein the metal film is composed of the same metal material as the electrode portion.

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#### REMARKS

Claims 2-5, 7-10, 12-20 and 22-25 are pending in the application. By this Amendment, claims 1, 6, 11 and 21 are canceled without prejudice or disclaimer and

claims 2, 4, 7-10, 12-17, 19, 20 and 22-25 are amended.

The Office Action indicates that the title of the invention is not descriptive. The title of the invention is changed as indicated above. The changed title is now believed to be descriptive of the invention.

The drawing figures are objected to under 37 CFR 1.83 (a). A Request for Approval Drawing Corrections is filed herewith proposing a red-line corrections to Figs. 3-5 to overcome the objection. Withdrawal of the objection is respectfully requested.

Claims 1, 2, 4-6, 9, 10 and 21 are rejected under 35U.S.C. 102 (b) has anticipated by Yoshida et al. (U.S. Patent No. 5, 821,625). The rejection is respectfully traversed.

Claims 2, 4, 9 and 10 are amended to depend from independent claim 7 which, for the reasons discussed below, is allowable over the applied art.

Claims 1, 6 and 21 are canceled and therefore the rejection as applied to these claims is now moot.

Withdrawal of the rejection is respectfully requested.

Claims 7, 8 and 22-25 are rejected under 35 U. S. C. 103 (a) as unpatentable over Yoshida. Claims 3 and 11-20 are rejected under 35 U. S. C. 103 (a) has unpatentable over Yoshida in view of the Fujimoto et al. (U.S. Patent No. 5,930,599). The rejections are respectfully traversed.

Yoshida discloses a chip-on-chip structure that has a first semiconductor chip 1 and a second semiconductor chip 5. The first and second semiconductor chips 1 and 5 are joined via a bump 4 which also establishes an electrical connection between the chips 1 and 5. An electro-conductive layer 7 is provided on an insulation layer 8 covering a surface of the second semiconductor chip 5. The electro-conductive layer 7 has an extended area or ground terminal 11, and therefore, the electro-conductive layer 7 can reduce the close talk noise between the chips 1 and 5. The ground terminal 11 of the electro-conductive layer 7 is coupled with an electrode pad 6 on the second semiconductor chip 5. Examples of materials for the bump 4 and the electro-conductive layer 7 include an Sn/Pd two-layer structure film.



Fujimoto discloses a semiconductor device that has a first semiconductor chip 10 and a second semiconductor chip 20 that is face-down bonded to the first semiconductor chip 10 and the up bumps 22. The first semiconductor chip 10 is die-bonded on a die pad 31 of a lead frame and a bonding pad 12 of the first semiconductor chip 10 is connected to an outer lead 32 of the lead frame via a bonding wire 32.

Claims 7 and 22-25 have been amended as independent claims. Claims 7 incorporates the features of claims 1 and 6. Claim 22 incorporates the features of claims 1, 6 and 7. Claim 23 includes the features of claims 11, 12 and 13. Claim 24 includes the features of claim 11, 14 and 15. Claim 25 includes the features of claims 11 and 16.

The inventions recited in claims 7, 15, 22 and 24 are distinguishable from the applied art in that the extension portion is extended outwardly from the shield portion on the surface of the semiconductor chip. According to the claimed structure, wire bonding is available to the extension portion to make an electrical connection. On the other hand, according to the structure of Yoshida, direct wire bonding to the ground terminal 11 is impossible because the ground terminal is extended just to the electrode pad 6. As recited in claims 7, 15, 22 and 24, the extension portion of the shield portion is extended beyond an edge of the second semiconductor chip.

The inventions recited in claims 13 and 23 are distinguishable from the applied art because none of the applied art discloses a heat dissipation structure as the claimed invention. In the claimed invention, a bonding wire is directly bonded to the heat conductive member provided between the first and second semiconductor chips. And, the bonding wire connects the heat conductive member to the heat sink. The claimed structure is advantageous in heat dissipation efficiency.

The inventions recited in claims 16 and 25 are also distinguishable from the applied art. Although Yoshida discloses an Sn/Pd two-layer structure film, this film is one film having two layer structure provided on one semiconductor chip. On the other hand, according to the claimed invention, two semiconductor chips to form a chip-on-

chip structure have metal films on their surfaces, respectively, and these metal films are disposed in contact with each other or bonded to each other. Thus, the structures of the claimed inventions and the applied art are different.

Claims 3 and 8 depend from claim 7 and include all of the features of claim 7. Claim 12 depends from claim 15 and includes all of the features of claim 15. Claims 14 and 17-20 depend from claim 13 and include all of the features of claim 13. For at least the reasons the independent claims are allowable, it is respectively submitted that the dependent claims are also allowable as well as for the features they recite.

Claim 11 is canceled and therefore the rejection as applied to claim 11 is now moot.

For at least the reasons discussed above, withdrawal of the rejection is respectfully requested.

In view of the foregoing, reconsideration of the application and allowance of the pending claims are respectfully requested. Should the Examiner believe anything further is desirable in order to place the application in even better condition for allowance, the Examiner is invited to contact Applicants' representative at the telephone number listed below.

Keiichi DEN  
Application No.: 09/702,870

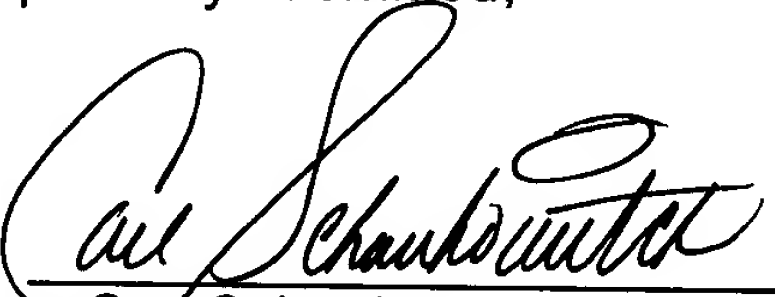
Attorney Docket No. ROH-030

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Please charge any fee deficiency or credit any over payment to Deposit Account No.18-0013 that is necessary to consider an appropriate response timely filed.

Respectfully submitted,

By:

  
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Enclosure(s):      Marked-Up Version of Amended Claims  
Request for Approval of Drawing Corrections

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